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REMARKS

Applicant has prepared a Substitute Specification, including claims, to correct idiomatic, typographical, and drafting errors in the specification as originally filed. A comparison version, generated automatically using Deltaview 2.7 software from Workshare Technology, Inc., is attached which shows changes made to the specification by underlining additions and bracketing deletions. A clean copy of the Substitute Specification has also been attached.

The Examiner is requested to accept the Substitute Specification to facilitate the processing of the application.

No new matter has been added.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the title:

INDUCTOR FOR SEMICONDUCTOR DEVICE AND METHOD OF MAKING [THE] SAME

In the claims:

Claims 25-48 are new.

INDUCTOR FOR SEMICONDUCTOR DEVICE AND METHOD OF MAKING [THE]SAME

This application claims priority to Korean patent applications No. 96-55392 filed November 19, 1996 and No. 97-60671 filed November 18, 1997 in the name of Samsung Electronics Co., Ltd.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to [a]semiconductor [device]devices, and [method of making the same. In particular]more particularly, [the present invention relates]to [a]semiconductor [device]devices including spiral inductors [for an integrated circuit]and a method of making the same.

2. Description of the [Prior]Related Art

In forming a semiconductor device, the use of individual devices such as transistors, resistors, inductors, etc. [are]is indispensable.[Among them] Of all these devices, [it is]inductors are typically the most difficult to make [the inductors]since they [are more]have the most complicated [in structure than other devices]structures.

[FIGs]FIGS.1 to 4 are perspective views for explaining a conventional method of making inductors in a semiconductor device[, which incorporates] as disclosed in U.S. Patent No. 3,614,554 ([Title of Invention :]"Miniaturized Thin Film Inductors For Use In Integrated Circuits", Application No. 770,375).

After collectors 13 of integrated circuits are formed in a semiconductor substrate 10 according to a design rule, the surface of the substrate is covered with a first insulating layer 12, and then conductive collector terminals 15 are formed which connect to the collectors 13. Then, after [a]first [to an]through eighth [underlying]lower conductive lines 14a to 14h constituting conductors are formed [of]using metal materials (FIG. 1), an oxide film 16 is formed to cover the surface of the substrate on which the first [to the]through eighth [underlying]lower conductive lines 14a to 14h are formed. Then,[and then] a bar 18 of magnetic [materials]material is formed [in order to cross]on top of the oxide film 16 and across the first [to the]through eighth [underlying]lower conductive lines 14a to 14h (FIG. 2).

Thereafter, a second insulating layer 20 is formed to cover the surface of the substrate on which the bar 18 is formed[, and then a first to a]. First through eighth contact

[hole]holes 22[a to]a to 22[h that expose]h are then formed in the insulating layer 20 thereby exposing one [ends of the first to]end of each of the first through eighth [underlying]lower conductive lines 14[a to 14h and a]a to 14h, and ninth [to a]through fifteenth contact [hole]holes 24[a to 24h that expose]a to 24h are formed so as to expose the other [ends of the first to the]ends of the first through eighth [underlying]lower conductive lines 14a to 14[h are formed on the second insulating layer 20.]h. Next, a layer of metal material is formed on the oxide film 16 to cover the contact holes[and]. The metal layer is then[is] patterned[, thereby forming a] to form upper conductive lines 26a through 26g. A first end of each of upper conductive lines 26a-26g is connected to a first end of each of lower conductive lines 14a-14g, respectively, through contact holes 22a-22g, respectively. A second end of each of upper conductive [line]lines 26a[which]-26g is connected to [the]a [one]second end of [the first underlying]each of lower conductive [line]lines 14[a]b-14h, respectively, through [the first]contact [hole 22a and is also connected to the other end of the second underlying conductive line 14b through the ninth contact hole 24a; a second upper conductive line 26b which is connected to the one end of the second underlying conductive line 14b through the second contact hole 22b and is also connected to the other end of the third underlying conductive line 14c through the tenth contact hole]holes 24[c; a third upper conductive line 26c which is connected to the one end of the third underlying conductive line 14c through the third contact hole 22c and is also connected to the other end of the fourth underlying conductive line 14d through the eleventh contact hole 24d; a fourth upper conductive line 26d which is connected to the one end of the fourth underlying conductive line 14d through the fourth contact hole 22d and is also connected to the other end of the fifth underlying conductive line 14e through the twelfth contact hole 24e; a fifth upper conductive line 26e which is connected to the one end of the fifth underlying conductive line 14e through the fifth contact hole 22e and is also connected to the other end of the sixth underlying conductive line 14f through the thirteenth contact hole 24f; a sixth upper conductive line 26f which is connected to the one end of the sixth underlying conductive line 14f through the sixth contact hole 22f and is also connected to the other end of the seventh underlying conductive line 14g through the fourteenth contact hole 24g; a seventh upper conductive line 26g which is connected to the one end of the seventh underlying conductive line 14g through the seventh contact hole 22g and is also connected to the other end of the eighth underlying conductive line 14]b-24h[through the fifteenth contact hole 24h; and a metal pad 30 connected to the one end of the eighth underlying conductive line 14h for applying an external signal (FIG], respectively. [4).]

[At this time, the]The first [to the]through eighth [underlying]lower conductive lines 14a to 14h and the first to the seventh upper conductive lines 26a to 26g [constitutes]form a single inductor coil.

FIG. 5 is a sectional view of a conventional conductor taken along line a-a' of FIG. 4, wherein the same reference numerals as those [explained by reference to FIGs]used in FIGS. 1 to 4 indicate the same components.

[The one]One end of the second [underlying]lower conductive line 14b is connected to the second upper conductive line 26b, and the other end thereof is connected to the first upper conductive line 26a.

[According to the above-referenced U.S. Patent No. 3,614,554, there]There are two disadvantages to an inductor fabricated as [follows.]described above.

[Firstly]First, when the line width of the conductive [line]lines of the inductor coil is [made fine]reduced, the[value of] self-[induction]inductance L [is reduced due to]of the [reasons]inductor is reduced as explained [in detail]below, even though the [thickness]thicknesses of the oxide film 16 and the second insulating layer 20 [is]remain constant.

In [case of]an inductor coil that is [winded]wound [in]with N [numbers]turns [on]around a magnetic material having a non-magnetic permeability of μ_S and a cross-sectional area of S,[when] current I [flows]flowing through the inductor [coil,]generates a magnetic field H[is generated], and the self-[induction]inductance L[of this time] is given [as]by Equation 1.

$$L = [N \quad sHS]N\mu_0\mu_S HS/I \quad [----------] \text{ (Equation 1)}$$

When [the]two inductors are [consisted]fabricated, the mutual inductance [value]is expressed [as]by Equation 2, wherein i is current, V is voltage, Φ is magnetic flux density, and n is the number of [winding]turns.

[---------- Equation 2]

$$M_{21} = n_2\Phi_{21}/i_1, \quad M_{21} = M_{12} = M, \quad V_1/V_2 = i_2/i_1 \quad \text{(Equation 2)}$$

[According to the above] From Equation [1,]1 it is apparent that the self-[induction]inductance L is proportional to the cross-sectional area S inside the coil. [Here, assuming]Assuming that the length of the semiconductor device 10 in a direction [in]parallel

[with]to the bar 18 is "a" and the vertical [directional]length of the contact hole is "b" (see b in FIG. 5), [it becomes]the cross-sectional area is S = a x b.

[At this time, according to the above-referenced]In a device fabricated as described above with reference to U.S. [Patent No.]Patent No. 3,614,554, the dimension "a" is related to the size of the design which the inductor occupies, and [the]"b" is determined by the sum of the [thickness]thicknesses of the oxide film 16 and the second insulating layer 20. However, even [though]when the [thickness]thicknesses of the oxide film 16 and the second insulating layer 20 [is]are held constant, reducing the["a" value may be depended upon the state of the inductor coil, wherein in case that the line] width of the [underlying conductive line and the]upper and lower conductive [line both constituting the inductor coil is fine]lines, for example, to less than 0.5 [m]um, can reduce the ["b"]value of L because, even though "a" may depend on the area the inductor occupies, the value of "b" is constrained since it is relatively dependent [on]upon the line width, and thus[it], functions as a factor [of]in reducing the [L]value of L.

[Secondly]Second, [This is]because [that]the inductor coil disclosed in the above-referenced U.S. [Patent No.]Patent No. 3,614,554 [is]does not [circularly winded. In other words, in case that the inductor coil is not]have a circular cross section, [a continuous change of]the magnetic field [cannot be made since an abrupt change of the magnetic field is generated]changes abruptly at the [portion where]sharp turns in the coil [is bent (see A]as shown at I in FIG. [5).]5.

SUMMARY OF THE INVENTION

It is an object of the present invention to solve the problems [involved in]associated with the prior art, and to provide a semiconductor device including inductors in which the self-inductance can [increase]be increased easily [the value of self-induction]and [is capable of maintaining the change of]in which the magnetic field changes uniformly.

It is another object of the present invention to provide the most suitable method of making the inductor.

In order to accomplish [the]these [above-]objects, a semiconductor device including inductors according to the present invention comprises: an insulating layer formed on a semiconductor substrate; a [semicircle columnar]groove having a semicircular cross-section formed in said insulating layer; a cylindrical insulator [formed on]aligned with said groove; and[inductors of a] spring[shape]-shaped inductors having [underlying]lower conductive

lines formed between said insulator and said groove[,] and[having] upper conductive lines [being]in [contacted]contact with the [underlying]lower conductive lines.

The lower conductive lines are slanted longitudinally along the groove and formed across the groove with a predetermined distance therebetween. The upper conductive lines are also slanted longitudinally along the groove and formed across the groove with a predetermined distance therebetween.

[The underlying conductive lines are slantly longitudinally formed with] ~~a predetermined distance therebetween~~[along the groove, the underlying]

The ends of the upper conductive lines [being formed across the groove, the upper]are connected to the ends of the lower conductive lines [are slantly longitudinally formed with a predetermined distance therebetween along the groove, the upper conductive lines being formed across]on both sides of the [groove.]

~~The upper conductive lines are~~ [formed to connect their one end with one end of the underlying conductive lines, respectively and to connect their other end with the other end of the underlying conductive lines, respectively.]cylindrical insulator.

The semiconductor substrate is [any one of]formed from either silicon [substrate]or [and]a compound semiconductor [substrate]such as gallium arsenide etc. The entire [surface]surfaces of the [underlying]lower conductive lines, except for the portions [connecting]which [with]contact the upper conductive lines, [is]are covered with an oxide film and an oxidization prevention layer, in that order.

A method of making a semiconductor device including inductors according to the present invention comprises the steps of; forming a [semicircle columnar]groove having a semicircular cross-section in an insulating layer on a semiconductor substrate; forming [underlying]lower conductive lines with a predetermined distance therebetween [on]in the groove; forming a cylindrical [insulating layer in the groove formed with]insulator above the [underlying]lower conductive lines and [on the surface of the substract]aligned with the groove; and forming upper conductive lines on the [insulating layer to]insulator and in contact with said [underlying]lower conductive lines.

The step of forming the groove further comprises the steps of: forming a nitride film on the insulating layer; forming a photosensitive film pattern for exposing the nitride film [for]to form a groove; etching the nitride film by using the photosensitive film pattern as a mask[to be exposed the insulating layer for forming the groove]; and etching the exposed insulating layer.

The [underlying]lower conductive lines are [slantly]formed across said groove and slanted longitudinally [formed]along [said groove to across]the groove.

A method of making a semiconductor device including inductors further comprises the steps of: forming an insulating layer on the surface of the [underlying]lower conductive

lines; covering the entire surface of the substrate [formed with the insulating layer]with an oxidization prevention layer; and burying a buried material between the conductive lines in the groove.

[buring bury material between the upper conductive lines in the groove.]

A method of making a semiconductor device including inductors further comprises[the] the step of forming [a]a contact region by etching the insulating layer and the [insulating layer and the]oxidization prevention layer for connecting[the underlying] the lower and [upper conductive lines after the buring]upper conductive lines.

The step[.]

[The step] of forming[the insulating layer comprises the] the insulating layer comprises the steps of[;]: laminating an oxidizable material on[the] the entire surface of[the] the substrate[to thereby be entirely buried the groove;]; and forming the insulating layer on the surface of the substrate and the [insulating layer on]groove by oxidization of the [surface of the substrate and the groove by oxidization of the oxidizable material.]oxidizable material.

The step of filling the groove with oxidizable materials further comprises the steps of: laminating oxidizable materials on the entire surface of the substrate to [thereby buried]bury the groove; and etching the oxidizable materials to fill only [in]the groove.

A semiconductor device including inductors according to the present invention comprises:[a] [semicircle]a groove having a semicircular cross-section formed in an insulating layer on a semiconductor substrate; a magnetic core [formed]aligned [on]with the groove; and inductors having a spring shape[and], the inductors having [underlying]lower conductive lines formed between the magnetic core and the groove, and upper conductive lines formed on the magnetic core to [thereby]contact [with]the [underlying]lower conductive lines. The [underlying]lower and upper conductive lines are formed of aluminum or copper having low resistance value. The oxide film is formed between the substrate and the [underlying]lower conductive lines, and between the [underlying]lower conductive lines and the upper conductive lines.

A method of making a semiconductor device including inductors comprises the steps of: forming a [semicircle]groove having a semicircular cross-section in an insulating layer on a semiconductor substrate; forming [underlying]lower conductive lines with a predetermined distance therebetween [to]across the groove; forming a magnetic core in the groove [formed with]over the [underlying]lower conductive lines; and forming upper conductive lines on the magnetic core, the upper conductive lines [being contacted with]contacting the [underlying]lower conductive lines.

The step of forming groove comprises the steps of; forming an oxide film as a relief region on the substrate; forming a silicon nitride layer and [an oxide film in]a high temperature oxide film in on the oxide film; forming a trench by etching the oxide film,

silicon nitride layer and [oxide film in]high temperature oxide film; forming an oxide film on the entire surface of the substrate; forming an[semicircle] groove having a semicircular cross-section by wet-etching the oxide film; and removing the oxide film, silicon nitride layer and [oxide film in]high temperature oxide film.

The step of forming [underlying]the lower conductive lines comprises the steps of[;]: forming an oxide film on the entire surface of the substrate; forming a conductive material on the oxide film; and forming [underlying]lower conductive lines with a predetermined distance therebetween along the groove by patternizing the conductive material.

The step of forming the magnetic core comprises the steps of[;]: forming an oxide film, a magnetic material and a capping oxide layer [in order on]over the [substrate formed with the underlying]lower conductive lines; forming the magnetic core in the groove by patternizing the magnetic material; and wrapping the magnetic core with the oxide film by forming a spacer at both [side]sides of the magnetic core.

BRIEF DESCRIPTION OF THE DRAWINGS

The above [object]objects, and other features and advantages of the present invention will become more apparent by describing the preferred embodiment thereof with reference to the accompanying drawings, in which:

[FIGs]FIGS.1 to 4 are perspective views for explaining a conventional method of making inductors [of]on a semiconductor device.

FIG. 5 is a sectional view of a conventional inductor taken along line [V]a-[V]a' of FIG. 4.

[FIGs]FIGS. 6A and 6B are a plan view and a sectional view, respectively, of a first embodiment of a semiconductor device including inductors, which is manufactured [by the method]in accordance with[a first embodiment of] the present invention.

[FIGs]FIGS. 7A to 12A and 7B to 12B are sectional views and plan views, respectively, for illustrating the process [flows]flow for [explaining the]a first embodiment of a method of making a semiconductor device including inductors according to[the first embodiment of the present invention, where respective process flows attached "A" are sectional views and respective process flows attached "B" are plan views.][FIG. 13A and 13B are a plan view and a sectional view of a semiconductor device including inductors, which is manufactured by the method in accordance with a second embodiment of] the present invention.

FIG. 13A and 13B are a plan view and a sectional view of a second embodiment of a semiconductor device including inductors, which is manufactured in accordance with of the present invention.

[FIGs]FIGS. 14A to 19[are]A and 14B to 19B are sectional views and plan views, respectively, for illustrating the process [flows]flow for [explaining the]a second embodiment of a method of making a semiconductor device including inductors according to the [second embodiment of the]present invention[, where respective process flows attached "A"]~~are sectional views and~~ [respective process flows attached "B" are plan views].

DETAILED DESCRIPTION[OF PREFERRED EMBODIMENTS]

[Fig]~~. 6A is a sectional view~~ FIG. 6B is a plan view of a first embodiment of a semiconductor device including inductors according to the [first embodiment of the]present invention, and [Fig. 6B is a plan view , where Fig. 6A is a plan view]FIG~~Fig.~~ 6A is a sectional view taken along line a-a' of [Fig]FIG.6B.

The semiconductor device [including inductors according to the first embodiment]of [the present invention, which comprises]FIGS. 6A and 6B includes a[semicircle columnar] groove having a semicircular cross-section 38 formed in an insulating layer 32 on a semiconductor substrate 30, [underlying]lower conductive lines 40[(40]a-40g (collectively "40") [longitudinally]formed [to intersect]across the groove 38 and slanted longitudinally with a predetermined distance [thereamong]therebetween along the groove 38, a cylindrical insulator 50 formed [on]above the lower conductive lines and aligned with the groove 38, an insulator 52 formed on the [smooth]flat part of the substrate, upper conductive lines 54a-54f [longitudinally](collectively "50") formed [to intersect]across the groove 38 and slanted longitudinally with a predetermined distance therebetween along the groove 38, and a magnetic core 47 formed [on]above the [underlying]lower conductive lines and below the insulator 50. The upper conductive lines 54a-54f [are arranged]slanted in the opposite direction [of]from the [underlying]lower conductive lines 40.

The semiconductor device [including inductors]of [the present invention]FIGS. 6A and 6B also [comprises]includes an oxide film 42 formed [on]over the [entire surface of the underlying]lower conductive lines 40a-40g except for the contact portion A, an oxidization prevention film 44 formed on all the surfaces of the substrate except for the contact portion A, a buried layer 46 buried in the groove [38]38, and [a]an oxide prevention film 56 formed over the entire semiconductor device on all surfaces of the substrate including the upper conductive lines 54.

[At this time, the underlying] The lower conductive lines 40 [are slantly arranged with the shortest line intersecting the groove 38 with the predetermined distance thereamong. The]and upper conductive lines 54 are [slantly arranged to the underlying conductive lines 40]slanted in [the]opposite [direction with a predetermined distance thereamong]directions so that [they]each of the upper lines are connected to one end of the two neighboring [underlying]lower conductive lines. That is, the first upper conductive line 54a is connected to one end of the first [underlying]lower conductive line 40a and one end of the second [underlying]lower conductive line 40b through [the]contact [portion]portions A. The second upper conductive line 54b is connected to one end of the second [underlying]lower conductive line 40b and one end of the third [underlying]lower conductive line 40c through the contact [portion]portions A. The [others of the]other upper conductive lines are connected to the [underlying]lower conductive lines, respectively, [as]in the same manner.

Therefore, both the upper conductive lines and the [underlying]lower conductive lines [are formed their connecting parts as]form a spiral coil unlike the prior art.

In the present invention, the [underlying]lower and upper conductive lines are made of polysilicon [into]doped [which]with impurities [are doped]and conductive materials such as tungsten T etc.[, and the] The semiconductor substrate 30 is made of a compound[,] such as [a]silicon (Si[or a]), gallium arsenide (GaAs), etc.

[Therefore, firstly, according to the inductors of]An inductor in accordance with the present invention solves problems associated with conventional inductors. First,[since] the self-inductance [value]of an inductor in accordance with the present invention is not dependent on[the length of] the vertical [direction]length of the contact hole for connecting the upper [conductive lines]and [the underlying]lower conductive lines, but [is]instead, [dependent]depends on the thickness of the insulator [50, the conventional problem can be solved that]50. Therefore, the self-inductance [value is relatively]is not dependent on the line width of the conductive lines [constituting]as with a [spiral]conventional [coil]inductor.

[Secondly]Also, since the [coil can be made]cross-sectional shape of an inductor in accordance with the present invention is more nearly circular[shape unlike the prior art], [both the underlying conductive lines and the upper conductive lines surround the insulators of a columnar shape, the conventional problem can be solved that a continuous change of magnetic field could not be made due to an]there are no abrupt [change]changes [of]in the magnetic field[generated at the portion] where the coil [is bent]bends (see I in FIG. 5).

[FIGs]FIGS. 7 to 12 are [process flows]views for [explaining]illustrating the process flow of a first embodiment of a method of making a semiconductor device including

inductors according to the present invention, wherein [respective process flows attached]the "A" figures are sectional views and [respective process flows attached]the "B" figures are plan views.

[First, FIGs]FIGS. 7A and 7B are [sectional]views showing the semiconductor device after the[semicircle columnar] groove 38 is formed. As can be seen from the drawings, a first insulating layer 32 is formed on a semiconductor substrate 30 made of [compound, such as a]silicon[or], gallium [arsenic]arsenide, etc., by depositing or growing[,] an oxide film 32 [with 10,000A of]to a thickness of 10,000Å. Subsequently, a silicon nitride layer 34 is formed [with 1,500A of]to a thickness of 1,500Å on the first insulating layer 32, and a photosensitive film pattern 36 is formed on the silicon nitride layer [34 to be]34. The ~~of~~ photosensitive film pattern is exposed [the silicon nitride layer placed in the portion]to form a pattern for [forming a semicircle columna]the groove. Next, the first insulating layer 32 is exposed by etching the exposed silicon nitride layer 34 using photosensitive film pattern 36 as [the]a mask[of]~~photosensitive film pattern~~ [36.]. Subsequently, the groove 38 is formed by etching the exposed first insulating layer[, in which the groove is to form the spiral inductor. At this time, the first insulating layer 32 is etched] by [the]a predetermined [manners,]process such as anisotropic etching[or], isotropic etching, or[the] combined [etching of]anisotropic [etching]and isotropic etching.

[FIGs]FIGS. 8A and 8B are [sectional]views showing the semiconductor device after [underlying]the lower conductive lines 40 and magnetic core are formed. The photosensitive film pattern 36 and a silicon nitride layer 34 are removed and a conductive material, for example, doped Poly-Si or Tungsten W is deposited on the entire surface of the substrate including the groove 38. The conductive material is patternized by a conventional method to [thereby]form the [underlying]lower conductive lines 40 [of]across the [inductor.]groove 38. The [underlying]lower conductive lines 40 are [slantly]slanted longitudinally [formed]along the groove 38 with a predetermined distance therebetween[along the groove 38. At this time, the underlying conductive lines 40 are formed across the groove 38. Subsequently]. Then, an oxide film 42 is formed[,] as a relief film[,] on the [underlying]lower conductive lines 40 [with 150A of]to a thickness of 150Å. At this time, the oxide film 42 is formed by [the manner in that]either oxidizing the surfaces of the [underlying]lower conductive lines 40[are oxidized]a-40g or depositing or growing the oxide film 42[is deposited or grown] on the [underlying]lower conductive lines 40a-40g. An [oxide]oxidation prevention layer 44, [such as]e.g., a nitride, is deposited [with 500A of]to a thickness [on]of 500Å over the entire surface of the substrate. [Next]Then, a buried layer 46 is formed in the gaps between the

[underlying]lower conductive lines 40 in the groove [38. In other words, by a]38 using an etchback process to form a flux material[,] such as[,] spin-on glass [GOS is formed with 2000A of]SOG to a thickness[to] of 2000Å thereby [being buried]burying the [underlying]lower conductive lines 40a-40g in the groove [38.]38 and then etching the flux material back until the oxdization prevention layer is exposed. [That is]Next, a core [materials]material, such as a magnetic [material]or conductive material, is formed on the entire [of the]substrate [with 1000A of]to a thickness of 1000Å and then limited to[thereafter be formed a magnetic core 47 only in] the groove 38 by wet or dry [pattering.]patterning, thereby forming a magnetic core 47.

[FIGs]FIGS. 9A and 9B are [sectional]views of the semiconductor device after [a semicircle columna groove is filled with]an oxidizable material [to thereby be smoothed a substrate. On the entire surface of the]is formed on the device. The groove and surrounding substrate [the]is covered with an oxidizable material 48, such as polysilicon or [armorphos]amorphous silicon [is formed with 10,000A of]to a thickness of 10,000Å, and the [substrate]oxidizable material is [smoothed by the performing of the]then flattened using a GMP [process]or etchback process. At this time, the oxidizable material 48 is [exposed]removed until the oxidization prevention layer 44 and the buried layer 46 are exposed. Therefore, the oxidizable material 48 is divided into two parts, a first relatively thicker portion 48a [fomed on]formed within, and filling, the concave portion of the groove [38]38, and a second relatively thinner portion 48b formed on [the smooth]the surrounding flat portion[of the substrate.] of the substrate.

[FIGs]FIGS. 10[A and]A and 10B are [sectional views after an insulator 50 is formed by the]views after insulators 50 and 52 are formed. An oxidization [process for the oxidizable material]process, which expands the volume each of the oxidization portions, is performed on the oxidizable material 48a, 48b[. The oxidizable materials 48], thereby forming a [and 48b are oxidized, to thereby form a]thick oxide film 50[by oxidization] by oxidization of [the]the silicon.[At this] [time, when the oxidization portion is oxidized, the volume thereof is expanded, and therefore the oxidization portion the]Since the expanded volume depends on the initial thickness[of which is thick forms a relative thicker insulator than an oxidization portion the], the cylindrical insulator 50 is formed to a thickness[of which is thin. In other words, a cylindrical insulator 50 is formed by means of the first oxidization portion, and peripheral insulators 52 the thickness of which are thinner than] that [of the insulator 50 are formed by means of the second oxidization portion.]is greater than that of the peripheral insulators 52.

At this time, the oxide prevention layer 44 is maintained [at]in an exposed state since it is not oxidized.

[FIGs]FIGS. 11A and 11B are [sectional]views after[a] contact [region]regions A for connecting the upper conductive lines (not illustrated) and [underlying]lower conductive [line]lines 40 are formed. The contact region A is formed[by removing]~~oxide films which might~~ [be formed on the oxidization prevention layer (indicated by 44 in FIG. 10)] by lightly wet-etching the resulting surface of the substrate [in which the insulator 50 and the peripheral insulators 52 are formed, and]including the oxidization prevention layer[, thus] 44 (and any ~~by removing~~ oxide films which might have formed thereon), thereby exposing the [underlying]lower conductive line 40.

[FIGs]FIGS. 12A and 12B are [sectional]views after the upper conductive lines 54 are formed. [The]A conductive material such as doped Poly-Si or Tungsten is formed[, as conductive material,] on the entire surface of the substrate[to], thereby [contact with]contacting the [underlying]lower conductive [line]lines 40 through [a]contact [region]regions A. Next, the upper conductive lines 54 are [longitudinary]formed across the cylindrical insulator 50 with a predetermined distance therebetween along the groove. The upper conductive lines 54 are formed by using a patternizing method [for]and slanted longitudinally along the [conductive materials. At this time,]insulator in the[upper conductive lines 54 are formed across the groove 38 to thereby be] opposite direction [of]from the [underlying]lower conductive lines 40a-40f. The upper conductive lines 54a-54f are formed [to contact their]such that both of their ends [with]contact [the]a neighboring [corresponding underlying]lower conductive [lines thereto]line through the contact [region]regions A.[Subsequently, on]

Next, an insulating material is formed over the entire semiconductor device on all surfaces of the substrate including the upper [conductive lines 54 insulating material is covered to]conductive lines 54, thereby [form]forming an insulating layer 56 [so that a]for protecting the cylindrical coil [consisted]consisting of the [underlying]lower and upper conductive lines[can be protected]. As shown in [Fig]FIG. 12B, one end of the first [underlying]lower conductive line 40a is connected to the one end of the upper conductive line 54a, and the other end of the upper conductive line 54a is connected to the other end of the [underlying]lower conductive line 40b. The [same]remaining conductive lines are connected in a similar manner[can be applied to the rest parts of the underlying and upper conductive lines].[Furthermore,] The insulator 50 assists the formation of a coil [is formed to have]having a spiral shape[by assistance of the insulator 50.] FIG. 13A and 13B are a plan view and a sectional view of a second embodiment of a semiconductor device including inductors[, which is] manufactured [by the method]in accordance with [a second embodiment of the]the present invention.

[FIGs. 14 to 19 are process flows for explaining the method of making a semiconductor device including inductors according to the second embodiment of the present invention, where respective process flows attached "A" are sectional views and respective process flows attached "B" are plan views.]

As shown in [Fig]FIG. 13A, a second embodiment of a semiconductor device including an inductor according to the present invention [comprises a semicircle columna]includes a groove having a semicircular cross-section 67 formed in an insulating layer 60 on [the]a semiconductor substrate[60, underlying], an oxide film 68 formed on the entire surface of the substrate including the inner surface of the groove, lower conductive lines [71(]71a-71g (collectively "71") [slantly]formed across the groove 67 and slanted longitudinally[arranged at a] along the groove with a predetermined distance therebetween[across the groove 67, an oxide film 72 formed on the entire of], an oxide film 72 formed over the entire surface of the [substrate 60 including the underlying]substrate including the lower conductive lines 71 to [thereby be exposed a predetermined surface of the underlying]conform to the surface of the lower conductive lines, a magnetic core 75 formed [on the oxide film 72 on the groove,]over the oxide film 72 and aligned with the groove, a capping oxide layer 76 formed over the top of the core 75, oxide spacers 78 formed along the sides of the core 75, upper conductive lines [54(54a-54]80a-80f (collectively "80") [slantly]formed across the magnetic core 75 and slanted longitudinally [formed]along the core with a predetermined distance therebetween[along the groove 38.]. The ends of upper conductive lines [54 are formed to]80 contact [their ends with the neighboring]the ends of corresponding [underlying]lower conductive lines 71[thereto] through [a]contact [region A.]regions C. Therefore, the upper and lower conductive lines formed a coil having a cross-sectional shape that is more nearly circular than a conventional coil.

[The semiconductor device according to the present invention] The semiconductor device of FIG. 14 further [comprises]includes a protection layer [86]82 formed on the entire surface of the substrate including the magnetic core 75 and the upper conductive lines [54.]80.

[At this time, the underlying conductive lines 71 are, as shown in Fig. 13B(71a-71g), consisted of a plurality of conductive lines which are formed to run counter with the nearest line acrossing the groove 100. Furthermore, the upper conductive lines are, as shown in Fig. 13B(80a-80f) consisted of a plurality of conductive lines which are formed to contact their ends with the ends of the neighboring corresponding underlying conductive lines thereto. Therefore, the underlying and upper conductive lines are formed to have a circular coil shape unlike the conventional method.]

[On the surface of the underlying conductive lines except for the connecting parts with the an oxide film 72.]The [underlying]lower and upper conductive lines [according to the present invention]71 and 80 are formed [by]from a conductive material[,] such as[the]

doped-polysilicon Poly-Si or tungsten T, and substrate [60]is made [of]from a compound[,] such as silicon or [galluim arsenic]gallium arsenide (GaAs).

[Therefore, according to] An inductor for a semiconductor device fabricated in accordance with the present invention as shown in FIG. 13 overcomes the problems[having] associated with conventional inductors because the[prior art can be solved since] self-inductance[value] does not depend the longitudinal length of the contact region for connecting the [underlying conductive lines and the]upper and lower conductive lines, but instead, depends on the thickness of the [insulator 50.] magnetic core 75. Furthermore, it is possible to form a circular coil since the [underlying and]upper and lower conductive lines are formed to enclose the [insulator.]core 75.

[FIGs] FIGS. [13]14 to 19 are [process flows]views for [explaining]illustrating the process flow of a second embodiment of a method of making a semiconductor device including inductors according to the [second embodiment of the]present invention, [where respective process flows attached]wherein the "A" figures are sectional views and [respective process flows attached]the "B" figures are plan views.[Figs. 14A, 14B and Fig. 15A, 15B are sectional views for forming a semicircle columna groove for a spiral coil.] [Figs]FIGS. 14A and 15A are sectional views taken along with the lines a-a' in FIGS. 14B and [a-a']15B, respectively.

[On a semiconductor substrate 60 made of compound, such as silicon] Referring to FIGS 14A and [Ga]14B, an oxide film 62 for relief is grown [with 500A of]on an insulating layer 60 to a thickness[and a] of 500Å. A silicon nitride layer 64 and [an oxide film in]a high temperature oxide film 66 are then formed [with 7000A of thickness.][Subsequently,]over the oxide film [66 in]62 to a thickness of 7000Å. The high temperature[,] oxide film 66, the silicon nitride layer 64 and the oxide film [62]62, are all etched [and]along with the [substrate]insulating layer 60 [is etched by]to a depth of 3 to 5μm of[thickness to] thereby [form]forming a trench 67a.

To form a groove having a [semicircle]semicircular [shape]cross-section, although it is not shown in the drawings, [the]an oxide film is grown in the trench 67a [is grown]to [thereafter be removed, and the oxide film is formed with 1μm of]a thickness [to thereby be]of 1μm and thereafter removed by wet etching. [And]Also, the[oxide film 66 in] high temperature[,] oxide film 66, the silicon nitride layer [64]64, and the oxide film 62 for relief are removed to thereby form a groove 67 having [the]a [semicircle]semicircular shape.

[Figs]FIGS. 15A and 15B are sectional views after the [underlying]lower conductive lines are formed. After [an oxide film 66 in]the high temperature[, a] oxide film 66, the silicon nitride layer [64]64, and [an]the oxide film 62 for relief are removed, an oxide film 68 is grown [with 2000A of]to a thickness of 2000Å for insulating an inductor [therefrom on]from the groove 67. Subsequently, a conductive material 70, such as [the]doped Poly-

Silicon[or], Aluminum or Copper [having low resistance value]is formed [with]to a thickness of 2μm[of thickness].

[Figs]FIGS. 16A and 16B are sectional views after the [underlying]lower conductive lines are formed. In [Figs]FIGS. 16A and 16B, [a]the conductive material 70 is patternized [by]using a photosensitive film pattern (not shown) to [thereby.]form [underlying]lower conductive lines 71(71a-71g)[.] across the groove 67. At this time, the [underlying]lower conductive lines 71 are [slantly]slanted longitudinally [formed]along the groove with a predetermined distance therebetween[along the groove 67 to thereby across the groove 67.].

An oxide layer 72 for insulating the [internal]interior of the inductor is formed [with 5000A of]to a thickness of 5000Å. [Subsequently, a]A core material 74, such as magnetic [material]or conductive material, is then formed on the oxide film 72 [to]and thereafter[be performed], a GMP process [for smoothing]is performed so as to flatten the core material. [Subsequently, a]A capping oxide layer 76 is then formed [with 5000A of]to a thickness of 5000Å on the surface of the [smoothed]core material [72.]74.

[Figs]FIGS. 17A and 17B are sectional views after a magnetic core is formed.

The magnetic core 75 is formed by patternizing both the core material 74 and the capping oxide layer 76 [by]using [the]a photosensitive film pattern (not shown). An oxide layer is then formed [with 5000A of]to a thickness [to]of 5000Å and thereafter[be anisotropic], anisotropicly-etched to [be]formed a spacer 78. Therefore, the magnetic core 75 is[definitely] isolated by the oxide films 72, 76 and 78.

[Figs]FIGS. 18A and 18B are sectional views after upper conductive lines are formed.

First, [an]the oxide film 72 is etched to form [a]contact [hole]holes C in order to [be exposed]expose both sides of each of the [underlying]lower conductive lines 71. The upper conductive lines 80(80a-80f) are then formed with the same conductive material as the [underlying]lower conductive lines.[At this time, the] The upper conductive lines 80 are [slantly]formed across the core 75 and slanted longitudinally [formed to across]along the [groove]core [67,]75 in the opposite direction [of]from the [underlying]lower conductive lines so as to [thereby]contact the [both]ends [thereof with]of the[neighboring] corresponding [underlying]lower conductive lines 71 [thereto]through the contact [hole]holes C.[Subsequently, on] An insulating material is then formed over the entire surface of the substrate [formed with]including the upper conductive lines 80 [is covered with insulating material]to[thereby] form an insulating layer 82. ~~Next, a metal wire 84 is formed~~[. The metal wire 84 is formed only at both ends of the underlying conductive lines if the inductor has a constant value, and may be formed every underlying conductive lines if the inductor has not a constant value.]

At this time, one end of the [underlying]lower conductive line 71a is connected to one end of the upper conductive line 80a. The other end of the upper conductive line 80a is

connected to the other end of the [underlying]lower conductive line 71b. The [same manner is applied to the rest parts of the underlying and upper]remaining conductive lines are connected in a similar manner.

Next, a metal wire 84 is formed at the lower conductive lines at both ends of the inductor to provide an electrical contact thereto. Wires can also be formed at other conductive wires to provide taps for obtaining different inductance values.

[Furthermore, it]It can be seen that a coil [consisting]formed [of]from the [underlying and]upper and lower conductive lines 71, [80]80, which are connected [therebetween]through the contact [hole]holes C [is formed to have]has a spiral shape.

[Figs]FIGS. 19A and 19B are a sectional view and plane view, respectively[according to the], of a third embodiment of the present invention.[In the drawings, the two] Two parallel grooves 67 are formed for an inductor which [is consisted of]includes upper conductive lines 80(80a-80g), 80[~]'(80a'-80g') and [underlying]lower conductive lines 71(71a-71g), 71'(71a'-71g'). It can [be]also be understood that the coil, which is [consisted of the underlying conductive lines and]formed from the upper and lower conductive lines[, is formed to have] has a spiral shape which does not have any angled portion caused by the insulator 50.

As described above, abrupt changes in the magnetic field of an inductor fabricated according to[the] the present invention[, the change of magnetic field] can be [constantly maintained]eliminated since the [inductors can be made]inductor has a spiral shape and the [increasement of]an increase in self-[induction value]inductance can [be]also be facilitated since the thickness of the insulator and the positional density of the conductive lines can be freely controlled.

While the present invention has been described and illustrated herein with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention.

INDUCTOR FOR SEMICONDUCTOR DEVICE **[INCLUDING INDUCTORS]**AND METHOD OF MAKING**[THE]** SAME

ABSTRACT OF THE DISCLOSURE

[There is disclosed inductors of a]An inductor for a semiconductor device[and method of making the same. The inductor according to the present invention includes a semicircle columnar groove] is formed within a groove in an insulating layer on a semiconductor [device,]substrate. [a]A number of [underlying]lower conductive lines are formed [on the insulating layer in the shape of intersecting]across the groove[, a columnar]. A cylindrical insulator is formed [on]over the [insulating layer so that the bottom face of which contacts the number of the]lower conductive lines[,] and[upper] aligned with the groove. Upper conductive lines [formed on the]are formed over the cylindrical insulator[in the shape of intersecting the insulator]. The upper and [connected to each of the number of the underlying]lower conductive lines[. As a result, according] are slanted lengthwise along the groove in opposite directions to [the present invention]form a spiral coil having a circular cross-section, thereby preventing abrupt changes in the[change of] magnetic field[can be maintained constant since the inductors can be made spiral and increase]. The ends of[self-induction can be also facilitated since] upper conductive lines contact the ends of the lower conductive lines so that the thickness of the [insulator]coil is controlled by the thickness of the cylindrical insulator, thereby allowing the self-inductance to be increased and the positional density of the conductive lines [can]to be freely controlled.